IN THE SPECIFICATION

[0003] FIG. 1A shows the typical structure of a prior art SOI device 10 prior to epitaxial Growth of the epitaxial, raised source/drain regions 28S/28D of FIG. 1B on the surface of the thin silicon layer 12 of the device 10. The device 10 includes a thin silicon layer 12 formed on a Buried OXide (BOX) layer 12. A gate electrode stack formed of dielectric (gate oxide) layer 14 upon is formed above the thin silicon layer 14, a gate electrode 18 composed of polysilicon formed above the gate dielectric layer 14, and a hard mask 22 above the gate electrode 18. ~~has been formed~~. Sidewall spacers 16 composed of silicon oxide have been formed on the sidewalls of the gate electrode 18 and are intended to cover the sidewall surfaces of the of the gate electrode 18 entirely.

[0005] FIG. 1B shows the device 10 of FIG. 1A after the epitaxial growth of the epitaxial raised source 28S and the epitaxial raised drain 28D on the surface of the thin silicon layer 12. The problem which is illustrated by FIG. 1B is that the exposure of the upper corners of the gate electrode 18 has led to spurious growth of epitaxial silicon nodules 28T [[is]] which are seen in the regions exposed at the top corners of the gate electrode 18 as shown on either side thereof.

[0006] The processing requirement in the past has been to protect the polysilicon of the gate polysilicon 18 with spacers 16 for the purpose of avoiding the formation of spurious epitaxial growth of such epitaxial silicon nodules during the formation.of epitaxial, raised source drain regions. ~~formation.~~

[0013] FIG. 1A shows the typical structure of a prior art SOI CMOS FET device before formation of the epitaxial, raised source/drain regions of FIG. 1B on top of the top surface of the thin silicon layer of the device.

[0014] FIG. 1B shows the device 10 of FIG. 1A after growth of the raised source and the raised drain by epitaxial growth of silicon on top of the top surface of the thin silicon layer with spurious growth of unwanted nodules at the upper corners of the gate electrode formed during the process of epitaxial growth.

[0019] Referring to FIGS. 2A and 2B, this invention provides a method for defining an epitaxial, raised source region 28S and an epitaxial, raised drain region 28D self-aligned with the gate electrode 18 and its sidewall spacers with a good process window. In particular, this invention provides a method/process for forming the structure of FIG. 1B without the growth of the spurious nodules 28T by protecting against the exposure of the polysilicon of the sidewalls of the gate electrode 18 to the epitaxial deposition process, which forms the epitaxial, raised source/drain regions 28S/28D over the top surface of the thin silicon layer 12.

[0020] The process requirement of the method of this invention is to insert an additional layer of dielectric material between the gate polysilicon of the gate electrode 18 and the spacers 26S for the purpose of eliminating the exposed polysilicon of the gate polysilicon of the gate electrode 18 and thereby avoiding the formation of spurious epitaxial growth during the formation of raised source/drain regions 28S/28D.

[0021] FIG. 2A shows the device 10 of FIG. 1A, which has been modified in accordance with this invention by forming an amorphous silicon layer 21 in the upper surface of the gate electrode 18 prior to forming the hard mask 22 on the top surface of the gate electrode 18, above the amorphous silicon layer 21. Then notches 24 (shown in FIGS. 3F and 3G) were formed at the top of the gate electrode 18 by etching away the outer edges of the amorphous silicon layer 21 as shown in FIGS. 3F and 3G. The notches 24 at the top of the gate electrode 18 were filled with dielectric plugs 26P thereby forming a Top Notched Gate (TNG) structure. The reason that the notches 24 were filled with the dielectric plug 26P was to prevent formation of the kinds of silicon nodules 28T seen in FIG. 1B on the polysilicon at the upper end of the gate electrode 18 as shown in FIGS. 3H and 3I.

[0022] FIGS. 2A and 2B are analogous to FIGS. 1A and 1B, showing the structure before and after the formation of the epitaxial, raised source/drain regions 28S/28D.

[0023] FIG. 2A shows spacer pull-down of spacers 26S extending down to the same level as shown by FIG. 1A, but the dielectric plug 26P prevents exposure of the polysilicon of the gate electrode 18 during the step of forming the epitaxial, raised source/drain regions 28S/28D on top of the top surface of the thin silicon layer 12. FIG. 2A shows the structure of the SOI device 10 in accordance with this invention, prior to epitaxial growth of the epitaxial, raised source/drain regions 28S/28D of FIG. 2B on the surface of the thin silicon layer 12 of the device 10. The device 10 includes a thin silicon layer 12 formed on a Buried OXide (BOX) layer 12. A gate electrode stack is formed on the thin silicon layer 12. The gate electrode stack includes a dielectric (gate oxide) layer 14 formed above the thin silicon layer 12; a gate electrode 18 composed of polysilicon above the gate dielectric layer 14; the notched amorphous silicon, cap layer 21 bordered by the dielectric plugs 26P formed on the upper surface the gate electrode 18; and the hard mask 22 covering the upper surfaces of the amorphous silicon, cap layer 21 and the upper surfaces of the dielectric plugs 26P. Sidewall spacers 26S, which are composed of silicon oxide, have been formed on the sidewalls of the gate electrode 18 which cover the sidewall surfaces of the gate electrode 18 entirely. The sidewall spacers 26S reach up high enough from the silicon layer 12 to overlap the edges of the dielectric plugs 26P. The amorphous silicon cap layer 21 and the dielectric plugs 26P are covered by the hard mask 22. In other words, the sidewall spacers 26S, which cover the sidewalls of the gate electrode 18, are contiguous with and overlap the outer edges of the dielectric plugs 26P, which fill the notches 24, as shown in FIGS. 3F and 3G. The dielectric plugs 26P are formed at the top of the gate electrode 18 by etching away the outer edges of amorphous silicon cap layer 21 thereby recessing the periphery of the amorphous silicon cap layer 21 as described below with reference to FIGS. 3H and 3I.

[0024] FIG. 2B shows the device 10 of FIG. 2A after formation of the epitaxial, raised source/drain regions 28S/28D over the top surface of the thin silicon layer 12 with the improvement that the epitaxial growth is only at the site of the epitaxial, raised source region 28S and the raised drain region[[s]] 28D. There is no spurious growth of epitaxial silicon nodules on the top corner of the poly-silicon of the gate electrode 18 of the kind seen in FIG. 1B adjacent to the dielectric plugs 26P during the formation of the epitaxial, raised source/drain regions 28S/28D. The tops of the sidewall spacers 26S, in addition to covering the sidewalls of the gate electrode 18, are contiguous with and overlap the outer edges of the dielectric plugs 26P .

[0026] Preparation for the selective ~~undercut~~ undercutting of a thin region at the top of the gate polysilicon of gate electrode 18 of FIGS. 2A and 2B must be done in a controlled and repeatable manner by forming an amorphous silicon layer 21B, FIG. 3B, in the surface of the polysilicon layer 18B of FIG. 3A which is to be formed into the gate electrode 18 of FIGS. 2A, 2B, 3I and 3J.

[0028] FIG. 3B shows the stack of FIG. 3A after the first step of the present invention leading to the formation of the TNG structure of this invention, which is to form a blanket, thin amorphous silicon layer 21B in the top surface of the blanket polysilicon layer $18B_1$ in the process of ion implantation of ions 21B into the top surface of the blanket polysilicon layer 18B provided for formation of the gate electrode 18. Germanium or silicon ions (21I) are implanted ~~to~~ with a dose sufficient to amorphize the desired thickness of the blanket polysilicon layer 18B. The thickness of the amorphous silicon layer 21B can be tailored by the choice of ion energy used.

[0032] FIG. 3F shows the device 10 of FIG. 3E after the TNG selective formation of the notches 24 in the amorphous silicon layer 21B of FIG. 3E. In this step, the notches 24 are formed as undercut notches 24 below outer edges of the hard mask 22 thereby forming a recessed ~~to form an~~ amorphous silicon cap layer 21 between the notches 24 and above the blanket gate electrode layer 18B. A step of selective undercutting of the amorphized layer 21B is performed to form the notched amorphous silicon cap layer 21 by a process of polysilicon RIE (described in detail below). In other words, an RIE etching process removes the peripheral portion of the amorphous silicon cap layer 21B to form recesses 24 at the edges thereof producing the notched amorphous silicon cap 21 which remains intact between the notches 24 and below the hard mask 22, which remains intact as shown in FIGS. 3E and 3F.

[0036] FIG. 3J shows the device of FIG. 3I after formation of the epitaxial, raised source/drain regions 28S/28D juxtaposed with the sidewall spacers 26S with no nodules formed at the top of the gate electrode 18 adjacent to the protective, dielectric plugs 26P during the epitaxial process used to form the epitaxial, raised source/drain regions 28S/28D above the top surface of the thin silicon layer 12. The problem that is illustrated by FIG. 1B has been overcome since there is no exposure of the upper corners of the gate electrode 18, so that there is no spurious growth of silicon nodules 28T. Thus, the top corners of the gate electrode 18 are protected.